REMARKS

Claim Rejections - 35 U.S.C. § 102 and § 103

The Examiner has rejected claims 30 and 36 under 35 USC 102(e) as being anticipated by Demirlioglu et al. (U.S. Patent No. 5,571,744). The Examiner has rejected claims 32 and 37 under 37 USC 103(a) as being unpatentable over Demirlioglu et al. ('744) in view of Moslehi (U.S.Patent No. 5,168,072). The Applicant respectfully traverses. The cited references fail to teach or render obvious, either individually or in combination, all of the elements of the Applicant's claims. In particular, the cited references fail to teach the element of independent claim 30 of forming a silicide layer having a third thickness on the semiconductor material films, the third thickness at least twice a sum of the first thickness of the gate electrode and the second thickness of the semiconductor material film formed on the gate electrode. In contrast, Demirlioglu fails to teach the thickness of the silicide layer 50 in the specification and Figure 12 illustrating the silicide layer 50 fails to illustrate the silicide layer 50 having a thickness at least twice the sum of the gate electrode 26 and the silicon germanium layer 36. Moslehi also fails to teach that the reacted refractory metal interconnect segment 100 (silicide) has a thickness at least twice the sum of the thicknesses of the lower semiconductor gate region 50 and the upper semiconductor gate region 88 (see Figure 19, for example.) Additionally, it is not obvious in light of the cited references to form the third thickness of the silicide layer of the Applicant's claimed invention to be at least twice the sum of the first thickness and the second thickness because neither Demirlioglu nor Moslehi

teach forming a low resistance gate electrode. The cited references also fail to teach the element of independent claim 30 of forming a pair of sidewall spacers having a height above the third thickness of the silicide layer on the semiconductor material film on the gate electrode. Also, it would not be obvious to form the sidewall spacers of Demirlioglu or Moslehi to have a height above the third thickness of the silicide layer because neither form a silicide layer as thick as the one claimed by the Applicant to necessitate the formation of sidewall spacers above the height of the thickness of the silicide layer to prevent bridging and shorting of the silicide layer on the gate electrode with the silicide layer on the source and drain regions.

Therefore, the Applicant respectfully submits that the cited references, either in individually or in combination, fail to teach or render obvious claim 30 and claims 32, 36, and 37 that depend upon and incorporate the limitations of independent claim 30.

Petition for Extension of Time Pursuant to 37 C.F.R. 1.136(a)

Applicant respectfully petitions pursuant to 37 CFR 1.136(a) for a two-month extension of time to file this response to the Office Action mailed April 7, 2004. The extended period is set to expire on September 7, 2004. A check in the amount of $420.00 is enclosed to cover the fee for a two-month extension of time.

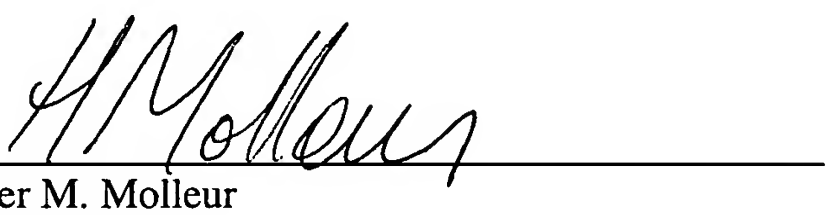
Pursuant to 37 CFR 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petititon for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 CFR 1.16 and 1.17, to Deposit Account No. 02-2666.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 9/7, 2004



Heather M. Molleur
Reg. No. 50,432

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300